

# UK Patent Application (12) GB (19) 2 315 920 (11) A (13)

(43) Date of A Publication 11.02.1998

(21) Application No 9715319.1

(22) Date of Filing 21.07.1997

(30) Priority Data

(31) 19630689

(32) 30.07.1996

(33) DE

(51) INT CL<sup>6</sup>

H01L 21/208 33/00

(52) UK CL (Edition P)

H1K KKAX KLDA K1EA K2S1C K2S1D K2S2D K2S20  
K2S23 K3E2 K3H K9E K9M2 K9N3

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(58) Field of Search

UK CL (Edition O) H1K KEAA KKAX KLDA

INT CL<sup>6</sup> H01L

Online:WPI,JAPIO,CLAIMS,INSPEC

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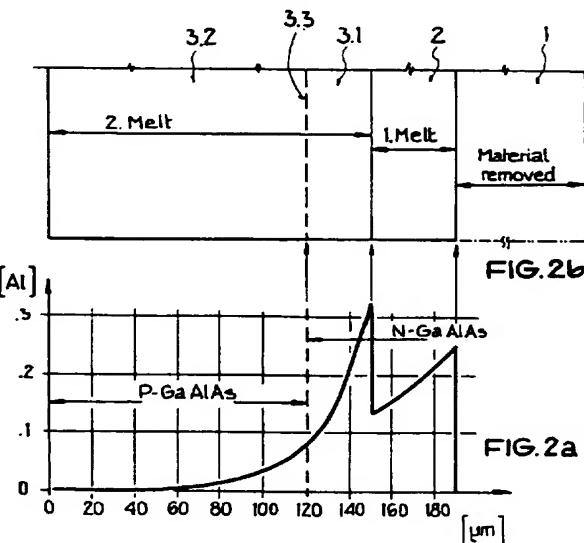
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## (54) Infra-red led

(57) A first GaAlAs-layer 3.2, 3.1 amphotERICALLY doped with silicon and comprising a p-conducting sub-layer 3.2 and an overlying, n-conducting sub-layer 3.1 wherein the Al-content continuously increases exponentially over the thickness of the whole of the first layer commencing from the surface side of the p-conducting sub-layer and amounts to approximately 0 atom-% on the surface side of the p-conducting sub-layer, approximately 5-10 atom-% in the zone of the pn-junction and approximately 25-40 atom-% on the surface side of the n-conducting sub-layer, and a second tellurium-doped, n-conducting GaAlAs-layer 2 arranged on the surface side of the n-conducting sub-layer of the first GaAlAs-layer 1, wherein the Al-content continuously increases exponentially over the thickness of the whole of the second layer commencing from the boundary surface to the first GaAlAs-layer and at the boundary surface to the first GaAlAs-layer amounts to approximately 6-16 atom-% but in any case is greater than in the zone of the p-junction, and at the surface amounts to at least 24 atom-% but at the maximum corresponds to the Al-content on the surface side of the n-conducting sub-layer. A process for the production of the semiconductor arrangement is also disclosed.



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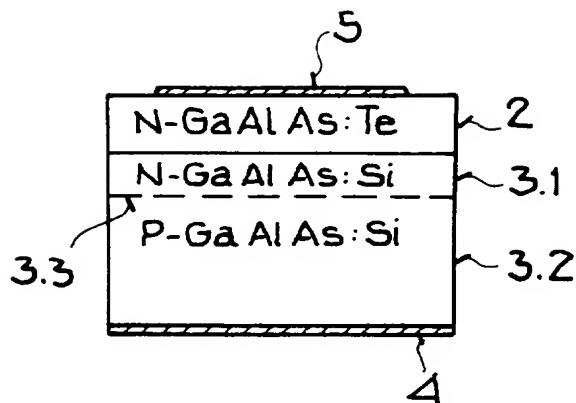


FIG. 1

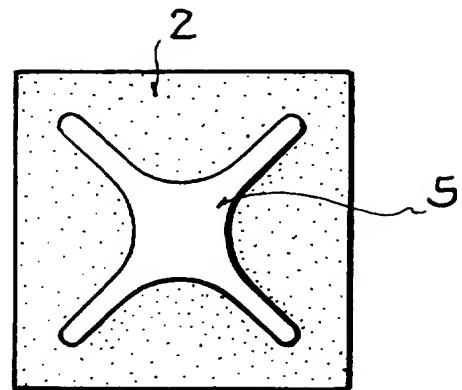


FIG. 3

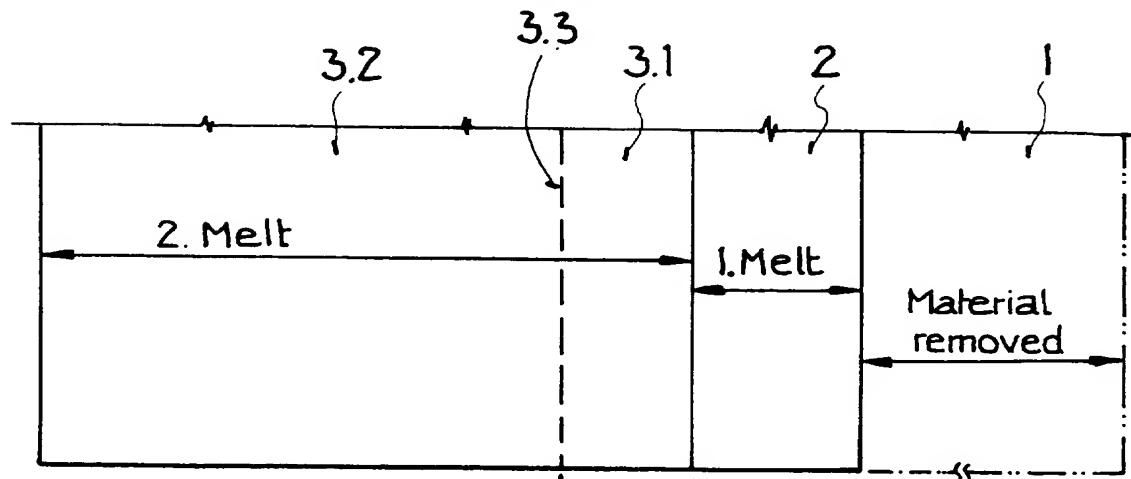


FIG. 2b

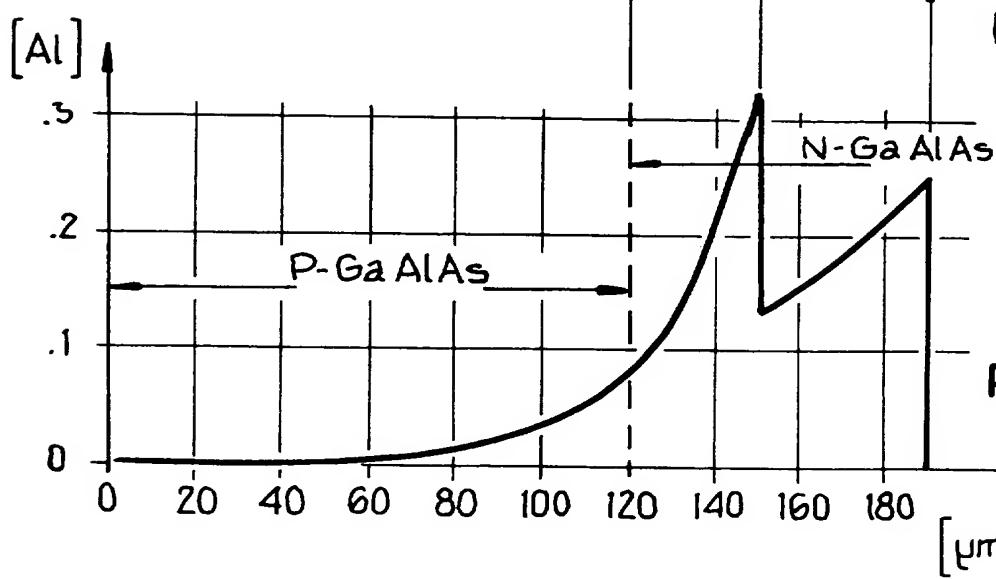


FIG. 2a

Semiconductor Arrangement

The invention relates to a semiconductor arrangement, in particular for a LED emitting infrared light, with a window layer which improves the light emission, and to a process for the production of such a semiconductor arrangement.

EP 0 356 037 A describes a process for the production of a LED with a double-hetero-structure. The following layers consisting of GaAlAs and having different aluminium constituents are produced consecutively on a GaAs substrate in the stated sequence from different melts. Firstly there is provided a p-conducting current propagation layer with an Al-content of 40 to 90 atom-%. The p-conducting current propagation layer is to distribute the current uniformly from the surface contacts onto the active layer. Then a p-conducting covering layer with an Al-content of 60 to 90 atom-% is formed. This is followed by the p-active layer with an aluminium content of 35 to 45 atom-%. The p-active layer forms a first heterojunction with the p-conducting covering layer. A n-conducting covering layer with an aluminium content of 60 to 90 atom-% is grown onto the p-active layer. The p-active layer forms a second heterojunction with the n-conducting covering layer. Finally a n-conducting, transparent carrier layer is formed on the n-conducting covering layer and the original substrate is removed. The n-conducting, transparent carrier layer is made as thick as possible in order to provide the semiconductor arrangement with adequate mechanical stability for the following process steps upon the separation of the diode chips and the mounting in the housings. The LEDs produced from this semiconductor arrangement have a very high luminous intensity. However, the production process is very complex and thus costly.

Gillessen and Schairer "Light-Emitting Diodes", Prentice-Hall International, 1987, p. 118 to 125 describes a process

for the production of a diode emitting infrared light with a so-called graded-band-gap structure. A GaAlAs-layer doped with silicon is grown on a GaAs substrate by a liquid phase epitaxy process. The composition and geometrical configuration of the melt are selected such that the aluminium content of the grown layer reduces continuously along the thickness in the direction of growth. The silicon contained in the melt is incorporated into the lattice as acceptor or donor as a function of the temperature of the melt, so that the light-generating pn-junction 3.3 of the LED is formed from only one melt at a specified temperature during the epitaxy process. Following the removal of the GaAs substrate, the contact layers are produced and structured. Then the diode chips are separated.

Due to the relatively simple structure, such a semiconductor arrangement can be produced in a favourable manner. LEDs with diode chips produced from these semiconductor arrangements have a lower luminous intensity compared to those with double-hetero-structures. Because of its high aluminium content, the one surface side of this semiconductor arrangement is difficult to provide with a contact.

The present invention seeks to provide a semiconductor arrangement for LEDs emitting infrared light, which arrangement is simple to produce but mechanically stable and from which LEDs with a high luminous intensity can be produced. The present invention also seeks to provide a process for the production of such a semiconductor arrangement.

According to a first aspect of the present invention, there is provided a semiconductor arrangement comprising a first GaAlAs-layer amphotERICALLY doped with silicon and comprising a p-conducting sub-layer and an overlying, n-conducting sub-layer, wherein the Al-content continuously

increases exponentially over the thickness of the whole of the first layer commencing from the surface side of the p-conducting sub-layer and amounts to approximately 0 atom-% on the surface side of the p-conducting sub-layer, approximately 5-10 atom-% in the zone of the pn-junction and approximately 25-40 atom-% on the surface side of the n-conducting sub-layer; and a second tellurium-doped, n-conducting GaAlAs-layer arranged on the surface side of the n-conducting sub-layer of the first GaAlAs-layer, wherein the Al-content continuously increases exponentially over the thickness of the whole of the second layer commencing from the boundary surface to the first GaAlAs-layer and at the boundary surface to the first GaAlAs-layer amounts to approximately 6-16 atom-% but in any case is greater than in the zone of the pn-junction and at the surface amounts to at least 24 atom-% but at the maximum corresponds to the Al-content on the surface side of the n-conducting sub-layer.

According to a second aspect of the present invention, there is provided a process for the production of a semiconductor arrangement comprising the following steps, in order:

- provision of a monocrystalline substrate wafer consisting of GaAs;
- growth of a second epitaxial layer consisting of n-conducting GaAlAs from the liquid phase of a first melt, wherein the Al-content continuously decreases exponentially over the thickness of the whole of the second epitaxial layer in the direction of growth and at the start of the epitaxial growth amounts to at least 24 atom-%;
- growth of a first epitaxial layer consisting of GaAlAs from the liquid phase of a second melt, wherein the Al-content continuously decreases exponentially over the thickness of the whole of the first epitaxial layer in the direction of growth and at the start of the epitaxial growth amounts to 25-40 atom-%, and the second melt is doped with silicon in such manner that

firstly a n-conducting sub-layer and later a p-conducting sub-layer grow, which sub-layers form and enclose a light-emitting pn-junction; and

- removal of the substrate by etching.

A preferred embodiment of the present invention will now be described, by way of example only, with reference to the accompanying drawings, of which:

Figure 1 is a cross-section through a LED chip produced from a semiconductor arrangement according to the invention;

Figure 2a shows the characteristic of the aluminium concentration as a function of the layer thickness in the semiconductor arrangement;

Figure 2b is a cross-section through the semiconductor arrangement;

Figure 3 is a view from above of the LED chip according to Figure 1.

In the following an exemplary embodiment of the invention will be explained making reference to the Figures.

Figure 1 is a cross-section through a LED chip which has been produced from a semiconductor arrangement according to the invention. The semiconductor arrangement comprises a first GaAlAs-layer 3.2, 3.1 amphotERICALLY doped with silicon. This first GaAlAs-layer is subdivided into a p-conducting sub-layer 3.2 and a n-conducting sub-layer 3.1. Arranged on the surface of the n-conducting sub-layer 3.1 is a second GaAlAs-layer 2 which is n-conducting, for example as a result of doping with tellurium (Te). Contact layers 4, 5 are arranged on the corresponding surface sides of the first and second GaAlAs-layer 2. The aluminium content of the two GaAlAs layers changes continuously and exponentially

over the thickness of the respective layer. The characteristic of the aluminium concentration as a function of the layer thickness is shown in Figure 2a in the form of a graph. Figure 2b shows the corresponding points in a cross-section through the semiconductor arrangement.

Viewed from the rear of the arrangement (from the surface of the p-conducting sub-layer 3.2) the aluminium content in the first GaAlAs-layer continuously increases exponentially from a value of approximately 0 atom-% up to a value of approximately 32 atom-%. This increase also continues without discontinuities over the light-generating pn-junction 3.3 so that the p-conducting sub-layer 3.2 and the n-conducting sub-layer 3.1 merge steplessly into one another in respect of the aluminium content.

At the pn-junction 3.3 the aluminium content amounts to approximately 8 atom-%, corresponding to a wavelength of the emitted light of approximately 880 nm. At the boundary surface to the second GaAlAs-layer 2 the aluminium content of the first layer 3.1 finally amounts to approximately 32 %. At this point the aluminium content jumps to approximately 13 atom-% in the second GaAlAs-layer 2. It is important that here more aluminium is incorporated into the crystal than in the zone of the pn-junction 3.3. Then the band gap is sufficiently large to prevent any noticeable absorption of the light generated at the pn-junction 3.3 so that the second GaAlAs-layer 2 is transparent to this light.

Also in the second layer 2 the aluminium content continuously increases exponentially towards the surface. At the surface it amounts to approximately 25 atom-%. Here it is important that on the one hand the aluminium content at the surface be kept as small as possible so that the layer can be provided with a good electric contact while on the other hand the production process, which will be described later, requires a minimum aluminium content at

this point. The stated 25 atom-% has proved particularly advantageous. In the case of the diode chip according to Figure 1 the surface of the p-conducting sub-layer 3.2 of the first GaAlAs-layer is provided with a whole-surface rear contact 4. As the aluminium content in this layer is smaller than at the pn-junction 3.3, this layer is not transparent to the light generated here. The light is thus absorbed and does not reach the rear contact 4. A structured front contact 5, as shown in Figure 3, is arranged on the surface of the second GaAlAs layer 2.

In pulsed operation with a pulse current of approximately 1.5 A, an infrared diode of this type emits a radiated power of approximately 300 mW with an emission wavelength of approximately 870 nm and a forward voltage of approximately 2.8 V. The diode is thus particularly suitable for remote-control purposes, photoelectric beam devices, optocouplers and data transmission, also in particular since it can be operated for example from a 3V battery consisting of two cells.

The described semiconductor arrangement is produced with the aid of liquid phase epitaxy processes. Firstly the second GaAlAs-layer 2 is grown from a first melt on the surface of a substrate wafer 1 consisting of GaAs. The composition and geometrical configuration of the melt and the temperature characteristic during the growth are selected such that the aluminium content changes along the thickness of the grown layer, as shown in Figure 2a. At the start of the growth, the aluminium content of the instantaneously growing layer amounts to approximately 25 atom-%. At the end of the growth the aluminium content has fallen to approximately 13 atom-% as the melt is rapidly depleted of aluminium. The melt additionally contains a dopant which renders the layer n-conducting. Tellurium (Te) has proved particularly advantageous for this purpose.

Then the first GaAlAs-layer 3.1, 3.2 is grown from a second melt onto the surface of the second GaAlAs-layer 2. The second melt contains silicon as dopant. Silicon has the property mentioned in the introduction that it is incorporated either as donor or as acceptor as a function of the temperature at which the growth of the GaAlAs-layer takes place. The pn-junction 3.3 can thus be produced from one melt simply by changing the growth temperature. Also in the case of the growth of the first GaAlAs-layer 3.1, 3.2, the composition and geometrical configuration of the melt are selected such that during the growth the aluminium content changes along the direction of growth in accordance with the characteristic shown in Figure 2a. During the growth of the approximately 150  $\mu\text{m}$  thick layer the aluminium content falls from approximately 32 atom-% to approximately 0 atom-%. At the pn-junction 3.3 the aluminium content amounts to approximately 8 atom-% whereas previously an approximately 30  $\mu\text{m}$  thick, n-conducting sub-layer 3.1 has grown. Due to the low aluminium content the p-conducting sub-layer 3.2 is not transparent to the light generated at the pn-junction 3.3.

When the two GaAlAs-layers 2; 3.1, 3.2 have grown, the substrate 1 is removed. A mixture of  $\text{NH}_4\text{OH}$  and  $\text{H}_2\text{O}_2$  is suitable as etching agent for this purpose. The boundary surface of the second GaAlAs-layer 2 to the substrate acts as etching boundary when the aluminium content at this boundary surface is greater than 24 atom-%. Then, under the influence of the etching agent, an oxide forms which is not soluble in the etching agent and which prevents the further attack of the etching agent.

Finally a whole-surface rear contact 4 is applied to the surface of the first GaAlAs-layer 3.2, which corresponds to the rear side of the later diode chip. The surface of the n-conducting, second GaAlAs-layer 2 is provided with structured contacts 5 as shown in Figure 3. Then the

arrangement is separated into diode chips which are finally mounted in housings.

The process is characterised by its simplicity and permits the production of diodes of high luminous intensity at a comparatively low outlay.

Claims

1. A semiconductor arrangement comprising a first GaAlAs-layer amphotERICALLY doped with silicon and comprising a p-conducting sub-layer and an overlying, n-conducting sub-layer, wherein the Al-content continuously increases exponentially over the thickness of the whole of the first layer commencing from the surface side of the p-conducting sub-layer and amounts to approximately 0 atom-% on the surface side of the p-conducting sub-layer, approximately 5-10 atom-% in the zone of the pn-junction and approximately 25-40 atom-% on the surface side of the n-conducting sub-layer; and a second tellurium-doped, n-conducting GaAlAs-layer arranged on the surface side of the n-conducting sub-layer of the first GaAlAs-layer, wherein the Al-content continuously increases exponentially over the thickness of the whole of the second layer commencing from the boundary surface to the first GaAlAs-layer and at the boundary surface to the first GaAlAs-layer amounts to approximately 6-16 atom-% but in any case is greater than in the zone of the pn-junction and at the surface amounts to at least 24 atom-% but at the maximum corresponds to the Al-content on the surface side of the n-conducting sub-layer.
2. A semiconductor arrangement according to Claim 1, wherein the thickness of the p-conducting sub-layer amounts to approximately 100-140  $\mu\text{m}$  and the thickness of the n-conducting sub-layer amounts to approximately 20-40  $\mu\text{m}$ .
3. A semiconductor arrangement according to Claim 1 or 2, wherein the thickness of the second GaAlAs-layer amounts to between 40  $\mu\text{m}$  and 60  $\mu\text{m}$ .
4. A semiconductor arrangement according to any of Claims 1 to 3, wherein the Al-content in the zone of the pn-junction amounts to approximately 8 atom-%.

5. A semiconductor arrangement according to any of Claims 1 to 4, wherein the rear of the p-conducting sub-layer of the first GaAlAs-layer is provided with a whole-surface contact.

6. A semiconductor arrangement according to any of Claims 1 to 5, wherein a structured front contact is arranged on the surface of the second, n-conducting GaAlAs-layer.

7. A semiconductor arrangement substantially as herein described with reference to the accompanying drawings.

8. A light emitting diode device comprising a semiconductor arrangement according to any preceding claim.

9. A process for the production of a semiconductor arrangement comprising the following steps, in order:

- provision of a monocrystalline substrate wafer consisting of GaAs;
- growth of a second epitaxial layer consisting of n-conducting GaAlAs from the liquid phase of a first melt, wherein the Al-content continuously decreases exponentially over the thickness of the whole of the second epitaxial layer in the direction of growth and at the start of the epitaxial growth amounts to at least 24 atom-%;
- growth of a first epitaxial layer consisting of GaAlAs from the liquid phase of a second melt, wherein the Al-content continuously decreases exponentially over the thickness of the whole of the first epitaxial layer in the direction of growth and at the start of the epitaxial growth amounts to 25-40 atom-%, and the second melt is doped with silicon in such manner that firstly a n-conducting sub-layer and later a p-conducting sub-layer grow, which sub-layers form and enclose a light-emitting pn-junction; and
- removal of the substrate by etching.

10. A process according to Claim 9, wherein the Al-content amounts to approximately 5-10 atom-% in the zone of the pn-junction.

11. A process according to Claim 9 or 10, wherein at the start of the epitaxial growth of the second epitaxial layer the Al-content corresponds at the maximum to the Al-content at the start of the epitaxial growth of the first epitaxial layer.

12. A process according to any of Claims 9 to 11, wherein the growth of the second epitaxial layer is terminated in the case of an Al-content which amounts to approximately 6-16 atom-% but in any case is greater than in the zone of the pn-junction.

13. A process according to any of Claims 9 to 12, wherein the first melt contains tellurium as dopant.

14. A process according to any of Claims 9 to 13, wherein the epitaxial growth of the first epitaxial layer takes place up to a total thickness of approximately 150  $\mu\text{m}$ , the thickness of the n-conducting sub-layer amounting to approximately 30  $\mu\text{m}$ .

15. A process according to any of Claims 9 to 14, wherein the Al-content of the first epitaxial layer has fallen to approximately 0 atom-% at the end of the growth.

16. A process according to any of Claims 9 to 15, wherein the substrate is removed by means of an etching solution consisting of  $\text{NH}_4\text{OH}$  and  $\text{H}_2\text{O}_2$ .

17. A process according to Claim 16, wherein the Al-content of the second epitaxial layer at the boundary surface to the substrate is selected such that the boundary surface terminates the etching attack upon the removal of

the substrate.

18. A process for the production of a semiconductor arrangement substantially as herein described with reference to the accompanying drawings.

19. A process according to any of claims 9 to 18 for the production of a light emitting diode device.



**Application No:** GB 9715319.1  
**Claims searched:** 1-19

**Examiner:** SJ Morgan  
**Date of search:** 24 October 1997

**Patents Act 1977**  
**Search Report under Section 17**

**Databases searched:**

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K(KEAA,KEBB,KKAX,KLDA)

Int Cl (Ed.6): H01L

Other: Online:WPI,JAPIO,CLAIMS,INSPEC

**Documents considered to be relevant:**

Category	Identity of document and relevant passage	Relevant to claims
A	EP 0 317 228 A2 (MITSUBISHI) See lines 9-21, column 4, in particular.	
A,&	EP 0 143 957 A1 (SIEMENS) See figure 1.	
A	US 5 525 539 (OPTO DIODE) See line 4, column 4 - line 5, column 5.	
A,&	US 4 606 780 (SIEMENS) See figure 1.	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.